B.C.A. (Part—I) Semester—I Examination 1ST3: DIGITAL TECHNIQUES—I

[Maximum Marks: 60] Time: Three Hours] **Note**:—(1) All questions are compulsory. (2) Draw diagrams wherever necessary. EITHER 1. (a) Explain with truth table: (i) NOR gate (ii) EX-NOR gate. 6 (b) Convert (3A.B)₁₆ into binary, octal and decimal numbers. 6 OR (p) Perform the following conversions: (i) $(105.5)_{10} = (x)$, (ii) $(AC.7)_{16} = (x)_{10}$ $(iii) (32.5)_8 (x)_{16}$ 6 (q) Subtract (11001)₂ from (10110)₂ using 2's complement method. 3 What is 1's complement of a binary number? Convert (11001101), into 1's complement number. EITHER 8 (a) Explain working of TTL NAND gate with neat diagram. (b) Define: (i) Fan-in, Fan-out (ii) Noise immunity. 4 OR 6 (p) Explain working of CMOS NOR gate. (q) Explain working of DTL logic gate (NAND). 6 EITHER (a) State and prove De-Morgan's theorems. 6 (b) Reduce the following equations using Boolean laws:

(ii) $AC + ABC + A\overline{C}$.

(i) $AB + \overline{A}BC + \overline{A}B + ABC$

OR

	(p)	Draw logic diagram of $Y = AB\overline{C} + AC + A\overline{B}C$. Reduce the above equation and deliging diagram.	lraw 6
	(q)	logic diagram. Simplify the following equation using K-map:	0
	(4)	$f(A, B, C, D) = \sum m(1, 1, 2, 3, 5, 7, 9, 10, 12).$	6
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4.	(a)	What is full adder? Explain working of full adder.	6
	(b)	Explain IC 74181 as ALU.	4
	(c)	State the difference between half adder and full adder.	2
	OR		
	(p)	Explain working of 4 bit parallel adder	6
	(q)	Explain action of full subtractor.	6
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5.	(a)	What is multiplexer? Explain working of 8: 1 multiplexer.	8
	(b)	Explain use of demultiplexer as decoder.	4
	OR		
	(p)	What is decoder "Explain 3: 8 decoder.	8
	(q)	State difference between multiplexer and demultiplexer.	4

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