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AS–1498

B.C.A. (Part—I) Semester—I Examination

DIGITAL TECHNIQUES—I

Paper—1 ST 3

Time : Three Hours] [Maximum Marks : 60

N.B. :— Draw neat diagrams wherever necessary.

EITHER

1. (A) Explain following gates with truth tables :

(i) AND gate

(ii) OR gate

(iii) NOT gate. 6

(B) Perform the following conversions :

(i) $(0.1256)_{10} \rightarrow (\ )_2 \rightarrow (\ )_8$

(ii) $(320.14)_8 \rightarrow (\ )_{10} \rightarrow (\ )_{16}$

(iii) $(7A.3B5)_{16} \rightarrow (\ )_2 \rightarrow (\ )_8$ 6

OR

(P) Why NAND and NOR gates are called universal gates ? Explain with examples. 6

(Q) Subtract following numbers using 2's complement method :

(i) $(101011)_2 - (101111)_2$

(ii) $(1101)_2 - (1001)_2$

(iii) $(100011)_2 - (000011)_2$ 6

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EITHER

2. (A) Explain the construction and working of TTL NAND gate. 6

(B) Explain CMOS inverter. 3

(C) Explain :

(i) Noise immunity

(ii) Propagation delay. 3

OR

(P) Draw 3-input DTL NAND gate and explain its working. 6

(Q) Differentiate between CMOS and TTL. 3

(R) Explain the terms :

(i) Fan-in

(ii) Fan-out. 3

EITHER

3. (A) State and prove De Morgan's theorem. 6

(B) Prove the following Boolean equations and draw the logic diagrams :

(i) $\overline{AB + BC + CA} = (\overline{A} + \overline{B}).(\overline{B} + \overline{C}).(\overline{C} + \overline{A})$

(ii) $\overline{(A + B)} = \overline{A}.\overline{B}$. 6

OR

(P) Reduce the following equation using K-map

$f(A, B, C, D) = \Sigma m(0, 1, 2, 8, 9, 10, 15)$. 5

(Q) State the following Boolean laws :

(i) Commutative law

(ii) Distributive law. 3

(R) Implement the following equation using logic gates :

$Y = \overline{A}\,B\,C\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,D$. 4

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EITHER

4. (A) Explain the working of full adder circuit with truth table. 6

(B) Draw logic diagrams of half and full subtracter. 6

OR

(P) Explain the construction and working of 4-bit parallel adder. 6

(Q) Explain controlled 4-bit parallel adder/subtractor with 2's complement method. 6

EITHER

5. (A) What is decoder ? Explain 2 : 4 decoder. 4

(B) What is demultiplexer ? Explain 1 : 16 demultiplexer. 4

(C) Differentiate between multiplexer and demultiplexer. 4

OR

(P) What is multiplexer ? Explain 4 : 1 multiplexer. 6

(Q) Explain 1 : 4 demultiplexer. 4

(R) Draw logic diagram of 3 : 8 decoder. 2

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