AU–185

B.C.A. (Part-I) Semester-I Examination

DIGITAL TECHNIQUES—I

Paper—1ST3

Time : Three Hours] [Maximum Marks : 60

**Note :—** Draw neat diagrams wherever necessary.

**EITHER**

1. (A) Explain binary and hexadecimal number systems with examples. 6

(B) Perform the following conversions :

(i) $(FCB)_{16} \rightarrow (\ ?\ )_{10} \rightarrow (\ ?\ )_{8}$

(ii) $(31.14)_{10} \rightarrow (\ ?\ )_{2} \rightarrow (\ ?\ )_{8}$

(iii) $(6F2D.12)_{16} \rightarrow (\ ?\ )_{2} \rightarrow (\ ?\ )_{8}$ 6

**OR**

(P) Explain AND, OR and NOT gates with truth tables and symbols. 6

(Q) Explain the subtraction using 2's complement method. 6

**EITHER**

2. (A) Explain the construction and working of TTL NAND gate. 6

(B) Explain the DTL logic with circuit diagram. 6

**OR**

(P) Explain the terms :

(i) Propagation delay

(ii) Noise immunity

(iii) Fan-in. 6

(Q) Explain the working of CMOS NAND gate. 6

**EITHER**

3. (A) State and prove DeMorgan's theorem. 6

(B) Prove that :

(i) $A + \overline{A}B = A + B$

(ii) $A + (BC) = (A + B) \cdot (A + C)$ 6

**OR**

(P) Draw the K-map and simplify the following Boolean expression :

$f(ABCD) = \Sigma m(0, 1, 3, 5, 7, 8, 10, 11, 13, 15)$. 6

(Q) Explain pair of 1's, quad of 1's and octet of 1's in K-map. 6

**EITHER**

4. (A) Explain half adder and full adder with logic diagram. 6

(B) Explain the working of full subtractor with logic diagram. 6

**OR**

(P) Explain the construction and working of 4-bit parallel adder. 6

(Q) Draw logic diagrams of 4-bit binary adder and explain. 6

**EITHER**

5. (A) What is decoder ? Explain 3 : 8 decoder with logic diagram. 6

(B) What is demultiplexer ? Explain 1 : 16 MUX. 6

**OR**

(P) What is multiplexer ? Explain 16 : 1 MUX. 6

(Q) Explain 4 : 16 decoder with logic diagram. 6