EITHER

5. (A) Explain the working of 2 : 4 decoder with neat diagram. 4

(B) What is multiplexer ? Explain 4:1 multiplexer. 6

(C) Draw logic diagram of 1:8 demultiplexer. 2

OR

(P) Explain 1:4 demultiplexer with neat logic diagram. 6

(Q) What is decoder ? Explain 3:8 decoder with logic diagram and truth table. 6

AR – 630

First Semester B. C. A. (Part – I) Examination

DIGITAL TECHNIQUES – I

Paper – 1 ST 3

P. Pages : 4

Time : Three Hours] [Max. Marks : 60

Note : Draw neat diagrams wherever necessary.

EITHER

1. (A) Draw truth table and explain the working of (i) EX–OR gate (ii) NAND gate. 6

(B) Perform the following conversions :

(i) $(0{\cdot}8125)_{10} \longrightarrow (\quad)_2$

(ii) $(123{\cdot}8125)_{10} \longrightarrow (\quad)_{16}$

(iii) $(173{\cdot}64)_8 \longrightarrow (\quad)_{10}$ 6

OR

(P) Explain with truth table :

(i) AND gate,

(ii) OR gate and

(iii) NOT gate. 6

(Q) Explain 1's and 2's complement method of subtraction of binary numbers with example. 6

EITHER

2. (A) Give the classification of logic families. 4

(B) Explain —

(i) Fan–in.

(ii) Fan–out.

(iii) Noise immunity.

(iv) Power dissipation. 8

OR

(P) Explain construction and working of ECL. 6

(Q) Explain the working of TTL NAND gate. 6

EITHER

3. (A) State Boolean commutative, Associative and distributive laws. 6

(B) Verify – $A + \overline{A}B = A + B$ using Boolean laws. 2

(C) Implement the following equation using logic gates :

$$Y = AB\overline{C} + \overline{AB} + \overline{AC} + \overline{A}\,\overline{B}C$$ 4

OR

(P) State and prove Demorgan's theorem. 6

(Q) Reduce the following equation using k–map :

$f(A, B, C, D) = \Sigma(0, 1, 2, 3, 4, 5, 6, 7, 9, 10, 15)$ 6

4. (A) Explain the working of half adder circuit with truth table. 4

(B) Explain the working of full adder and full subtractor. 8

OR

(P) Explain the four bit parallel adder with example. 6

(Q) Explain IC 74181 ALU with neat diagram. 6