AT - 424

First Semester B. C. A. (Part - I) Examination

DIGITAL TECHNIQUES - I

Paper - 1 ST 3

P. Pages: 4

Time: Three Hours | [Max. Marks: 60]

Note: Draw neat diagrams wherever necessary.

EITHER

1. (A) What is Radix/Base of number system? Explain with examples. 3

(B) Convert

(i)
$$(100101)_2 \rightarrow (?)_{10}$$

(ii)
$$(37.125)_{10} \rightarrow (?)_2 \rightarrow (?)_8$$
 5

(C) Perform the following Additions:—

OR

(P) Define logic gate. Which are basic gates?

Draw its symbol.

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(Q) Why NAND and NOR gates are called

		universal gates? Explain. 4
	(R)	Explain substraction using 2's complement method with examples. 4
	EIT	HER
2.	(A)	State the classification of logic family. 3
	(B)	Explain the characteristics of logic family
		(i) Fan – in
		(ii) Fanout
		(iii) Noise immunity. 3
	(C)	Explain the construction and working of CMOS NAND gate. 6
		OR
	(P)	Explain DTL logic with circuit diagram. 6
	(Q)	Explain the working of TTL NAND gate. 6
	EIT	HER
3.	(A)	Explain K-map for two, three and four variables.
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(B) State and prove De Morgan's theorem. 6

OR

- (P) Reduce the following equation using K-map $f(A,B,C,D) = \sum m(1,5,6,7,11,12,13,15)$ and implement the final equation using logic gates.
- (Q) Prove the following Boolean equations and draw logic diagrams

(i)
$$ABC + A\overline{B}C + AB\overline{C} = A(B + C)$$

(ii)
$$\overline{\overline{A} \cdot \overline{B}} + A \cdot B = A \cdot \overline{B} + B \cdot \overline{A}$$
. 6

EITHER

- 4. (A) Explain with neat diagram 4-bit parallel Adder.
 - (B) Explain half subtractor with logic diagram.

OR

- (P) Explain full adder with logic diagram. 6
- (Q) Explain construction and working of 4-bit parallel adder/subtractor with 2's complement method.

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EITHER

5.	(A)	What is	decoder	.)	Explain	3:8	decoder	with
		logic di		6				

(B) What is demultiplexer? Explain 1:16 demultiplexer.

OR

(P)	What	is	multiplexer	?	Explain	16:1	MUX.
							6

(Q) Explain 4:16 decoder. 6

