AM–222

B.C.A Part–I (Semester–I) Examination
DIGITAL TECHNIQUES – 1ST3

Time : Three Hours]   [Maximum Marks : 60

Note :   (1) ALL questions are compulsory.

(2) Draw diagrams wherever necessary.

EITHER

1.   (A) What is Logic Gates ? Explain truth table and symbol of NOR and EX-NOR gate.   6

(B) Convert $(26.6)_{10}$ into Binary, Octal and Hexadecimal number system. .   6

OR

(P) Perform the following conversion and find the value of x :

(i) $(2013)_8 \rightarrow (x)_2$

(ii) $(AB.CF)_{16} \rightarrow (x)_8$

(iii) $(111010.0110)_2 \rightarrow (x)_{16}$.   6

(Q) Subtract $(1010)_2$ from $(1101)_2$ using 1's and 2's complement method.   4

(R) Draw the symbol of NAND and EX-OR gate. 2

EITHER

2.   (A) What is CMOS logic ? Explain construction and working of two input CMOS NAND gate.   8

(B) Define the terms :
   (i) Fan-in
   (ii) Fan-out
   (iii) Propagation delay
   (iv) Noise immunity.   4

OR

(P) Draw the circuit diagram of two input TTL NAND gate. Explain its construction and working.   8

(Q) State the specification and application of DTL NAND gate.   4

EITHER

3. (A) State and prove first and second De-Morgan's theorems using truth table.   6

   (B) Simplify the following Boolean equation :

   (i) $y = ABC + A\bar{B}C + AB\bar{C}$

   (ii) $y = AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC + ABC + A\bar{B}C$.   6

OR

(P) Draw the logic diagram and truth table for Boolean equation $y = A + \bar{A}B + A\bar{B}$.   6

(Q) Draw k-map and simplify the following Boolean equation :
   $f(A, B, C, D) = \Sigma m\ (0, 2, 4, 6, 8, 10)$.   6

EITHER

4. (A) What is Half adder ? Explain the construction and working of half adder.   6

   (B) Draw the logic diagram of 4 bit parallel adder.   3

   (C) State the difference between half adder and full adder.   3

OR

(P) Explain the construction and working of full subtractor.   6

(Q) Explain the IC 74181 as ALU.   3

(R) Draw the logic diagram of full adder.   3

EITHER

5. (A) What is Demultiplexer ? Explain the construction of 1 : 4 demultiplexer with logic diagram and truth table.   8

   (B) Explain use of Decoder as Demultiplexer.   4

OR

(P) What is Decoder ? Explain construction of 2 : 4 decoder with logical diagram and truth table.   8

(Q) State the difference between Multiplexer and Demultiplexer.   4