9,	(A)	What is multiplexer? Explain 4:1 multiplexer.				AL-5
- 		Explain 3:8 decoder with logic diagram. 4				First Semester B. C. A. (Part-1) Examination DIGITAL TECHNIQUES - I
-	(C)	Draw logic diagram of 1:4 demultiplexer.			4.	Paper - 1 ST 3
		OR	**.	, ,		P. Pages: 4 Time: Three Hours] [Max. Marks:
10.	(P)	What is decoder? Explain 4:16 decoder.	•		5	Note: (1) All questions are compulsory. (2) Draw well labelled diagrams where
	(Q)	Explain 16:1 multiplexer with logic diagram.			*,	necessary
-			. I.			 (A) Explain conversion of octal to hexa deciment with the help of examples.
P			- 1			(B) Perform the following subtractions using land 2's complement methods:—
				-		(i) 101011 ₂ - 100110 ₂
	-			i,a i	٠.	(ii) 110011 ₂ - 101111 ₂

OR

(iii) 100011₂ - 10001₂

(P) Why are NAND and NOR gates called Universal gates? Explain with examples. 6

(Q) Perform the following :-

- (i) $(AA)_{16} = ()_{10}$
- $(ii) (77)_8 = ()_2$
- $(iii) (99)_{10} = ()_{8}$

3. (A) Explain :--

- (i) Fan-in, Fan-out.
- (ii) Noise immunity.
- (B) Explain construction and working of ECL.
- (C) What is meant by totem pole output ? 2

OR

- 4. (P) State classification of logic families. 3
 - (Q) Draw circuit diagram of DTL and explain working. 6
 - (R) Explain working of CMOS inverter.
- 5. (A) State and prove DeMorgan's theorems.
 - (B) Reduce the following equation and draw logic diagram.

 $Y = AB + A\overline{BC} + BC + \overline{AB}C + ABC$ 4

(C) What are SOP and POS terms ?

OR

6. (P) Minimize

 $f(A, B, C, D) = \Sigma m(0, 1, 2, 4, 8, 9, 14, 15)$

 Explain how truth table can be converted into standard SOP form with the help of example.

(R) Draw logic diagram of -

 $Y = A \overline{BC} + \overline{AC} + ABC + BC$ 2

 (A) Draw logic diagram of half adder and explain working.

(B) Describe ALUIC – 74181.

(C) Explain Pull substractor with the help of logic diagram.

OR

 (P) Explain Full adder with help of logic diagram and truth table.

(Q) Draw logic diagram of controlled parallel adder and explain its action.

(R) Draw logic diagram of 4-bit binary adder.

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