B.E. Eighth Semester (Electronics Engineering) (CGS)

# 10700 : VLSI Design : 8 XN 03

P. Pages : 2 | AU - 3004

Time : Three Hours | Max. Marks : 80

* 0 6 7 9 *

Notes : 1. Assume suitable data wherever necessary.
2. Illustrate your answer necessary with the help of neat sketches.

## SECTION – A

**1.** a) Explain static-1 hazard & how in can be avoided with suitable example. **7**

b) Implement the following expression using a multiplexer. **6**
$f(A,B,C,D) = \sum m(0,2,3,6,8,9,11,12,14)$.

**OR**

**2.** a) What are the different types of finite state machine (FSM) and its differences? Design a FSM for 1011 sequence. **7**

b) What are the difference between combinational and sequential circuit. **6**

**3.** a) Explain different types of objects in VHDL with example. **6**

b) Write a VHDL code for 4 : 2 priority encoder. **7**

**OR**

**4.** a) Write a VHDL code 5 :1 mux using CASE statement. **6**

b) Write a VHDL code for T-flip-flop with synchronous reset. **7**

**5.** a) When subprograms and packages are used in VHDL program? Explain with suitable example. **7**

b) Design and write a VHDL code for 4:1 mux using 2 : 1 mux as component is structural modeling. **7**

**OR**

**6.** a) Explain library IEEE? How to create user defined library. **7**

b) Design and write a VHDL code for n-bit parallel in serial out shift registers using generic statement. **7**

## SECTION – B

**7.** a) Explain input/output block and interconnect block of FPGA. **7**

b) Explain switch matrix block of CPLD. **6**

**OR**

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| **8.** | a) | Explain function block of CPLD 95XX. | **7** |
| | b) | Explain CLB & LUT block of FPGA architecture. | **6** |
| **9.** | a) | Explain why PMOS is used in pull-up and NMOS in pull-down network of CMOS design? Justify with proper equation. | **7** |
| | b) | Explain static and dynamic power dissipation on CMOS. | **7** |

**OR**

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| **10.** | a) | Design a CMOS circuit for the equation $\overline{(A \cdot B \cdot C) + D}$. | **7** |
| | b) | Explain the CMOS inverter dc transfer characteristics elaborating on various operating regions. | **7** |
| **11.** | a) | Write a VHDL code for an sequence 1101 detection using finite state machine. | **7** |
| | b) | Explain twin tub process in CMOS fabrication technology. | **6** |

**OR**

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| **12.** | a) | Write a VHDL test bench for D-flip flop verification. | **6** |
| | b) | Explain n-well process in CMOS fabrication technology. | **7** |

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