B.E. Fourth Semester (Electronics & Telecommunication) (New)

Digital Electronics : 4 ET 04

P. Pages : 2 | **AU - 2590**

Time : | Max. Marks : 80

* 0 9 6 9 *

Notes : 1. All question carry equal marks.
2. Answer **three** question from section A and **three** question from section B.
3. Assume suitable date wherever necessary.
4. Illustrate your answer necessary with the help of neat sketches.
5. Use of pen Blue/Black ink/refill only for writing book.

1. a) Explain in brief Transistor-Transistor logic (TTL) circuit with active pull up arrangements. Verify the logic operations given by TTL. **7**

b) Perform the following. **7**
i) Convert $(1011011)_2$ to Gray code
ii) Convert $(28F)_{16}$ to octal
iii) $(75)_{10}$ - $(57)_{10}$ by 2's complement method.

OR

2. a) Minimize the following logical expressions by Boolean Algebra **8**
i) $B \oplus (B \oplus AC) = AC$
ii) $ABC + B\bar{C}D + \bar{A}BC = BC + BD$

b) Explain the following characteristics of digital IC's. **6**
i) Noise Margin
ii) Figure of merit
iii) Fanin and Fanout

3. a) Minimize the following logic function and realize using NAND gates only. **7**
$f_1 (A, B, C, D) = \Sigma m (1,3,5,8,9,11,15) + d(2,13)$

b) Design the combinational circuit for full adder and implement it using suitable gates. **6**

OR

4. a) Design and explain one digit BCD adder circuit using 4-bit adder IC 74LS83 and required gates. Explain with the help of suitable example. **7**

b) Design binary to gray cod converter circuit using suitable gates. **6**

5. a) Implement the following logical expression using 8:1 MUX **7**
$F = \Sigma m (0,1,2,3,4,10,11,14,15)$

b) Design 5-line to 32 line decoder circuit using 4-line to 16-line decoders and suitable gate. **6**

OR

6. a) Design 5-bit comparator using single 7485 IC and suitable gate. Also explain its operation. **7**

b) Compare ROM, PLA and PAL **6**

7. a) What is Race around condition? How it is overcome? Explain master-slave J-K flip flop with proper table. 7

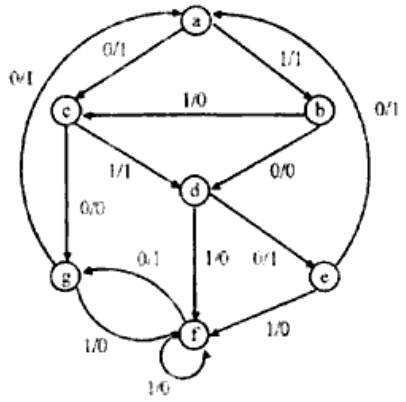
b) Design 4-bit parallel in serial out right shift register using D-Flip Flops and suitable gates. 6

OR

8. a) State differences between synchronous and asynchronous counters. 5

b) Design 2-bits asynchronous up counter using negative edge triggered T-Flip Flops and explain its operation with proper wave forms. 8

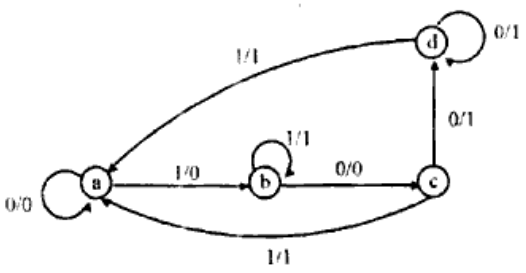
9. a) Obtain reduced state table and reduced state diagram for the sequential machine whose state diagram is shown below. 6



b) Draw the state diagram and state table for a Moore type sequence detector to detect the sequence 110. 8

OR

10. Design a clocked sequential circuit using T-Flip Flops and suitable gates for the state diagram given below. 13



11. a) Explain in brief- 8

i) PROM ii) EPROM

iii) EEPROM iv) NVRAM

b) Explain the working of dynamic RAM cell. 5

OR

12. a) Explain the read cycle timing parameters of a memory using proper timing diagram. 6

b) With neat circuit diagram explain the operation of bipolar static RAM cell. 7

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