AU – 2871

Seventh Semester B. E. (Electronics and Tele. Engineering) Examination

COMPUTER ORGANIZATION

Elective - I

Paper – 7 XT 04

(USC – 10631)

P. Pages : 4

Time : Three Hours] [Max. Marks : 80

Note : (1) Due credit will be given to neatness and adequate dimensions.
(2) Assume suitable data wherever necessary.
(3) Use pen of Blue/Black ink/refill only for writing the answer book.

1. (A) Draw the block diagram for Computer Components (Top Level View) and explain the function of each. 7

   (B) Consider a hypothetical 32 - bit microprocessor having 32 - bits instructions composed of two fields : The first byte contains the opcode and remainder the immediate operand or an operand address.

   (a) What is the maximum directly addressable memory capacity (in bytes)?

   (b) Discuss the impact on the system speed if the microprocessor bus has a 32 - bit local address bus and a 16 - bit local data bus or a 16 - bit local address bus and a 16 - bit local data bus. 7

OR

2. (A) List and briefly define the functional groups of signal lines for PCI. 7

   (B) Consider two microprocessors having 8 and 16 - bit - wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

   (a) Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ ?

   (b) Repeat assuming that half of the operands and instructions are one byte long. 7

3. (A) Explain the advantages and disadvantages of programmed and interrupt driven I/O. 7

(B) Consider a microprocessor that has a block I/O transfer instruction such as that found on the Z 8000. Following its first execution, such an instruction takes five clock cycles to execute. However, if we employ a non - block I/O instruction, it takes a total of 20 clock cycles for fetching and execution. Calculate the increase in speed with the block I/O instruction when transferring blocks of 128 bytes. 6

OR

4. (A) In virtually all systems that include DMA modules, DMA access to main memory is given priority than CPU access to main memory. Why ? 7

(B) A DMA controller servers four receive - only telecommunication links (One per DMA channel) having a speed of 64 Kbps each.

(a) Would you operate the controller in burst mode or in cycle stealing mode ?

(b) What priority scheme would you employ for service of the DMA channels ? 6

5. (A) What general roles are performed by processor register ? Explain. 6

(B) A microprocessor provides an instruction capable of moving a string of bytes from one area of memory to another. The fetching and initial decoding of the instruction takes 10 clock cycles. Thereafter, it takes 15 clock cycles to transfer each byte. The microprocessor is clocked at a rate of 5 GHz.

(a) Determine the length of the instruction cycle for the case of a string of 64 bytes.

(b) What is the worst-case delay for acknowledge an interrupted at the instruction is non-interruptible ?

(c) Repeat part (b) assuming the instruction can be interrupted at the beginning of each byte transfer ? 7

OR

6. (A) One limitation of the multiple - stream approach to dealing with branches in a pipeline is that additional branches will be encountered before the first branch is resolved. Suggested two additional limitations or drawbacks. 7

(B) Explain the following addressing modes using suitable example :—

(i) Immediate.

(ii) Indirect.

(iii) Direct. 6

7. (A) Explain the compiler based register optimization in detail with the help of time sequences of active use of registers and register interface graph. 7

(B) Differentiate between characteristics of RISC and CISC. 7

OR

8. (A) Draw the architecture of power PC 620 and explain the details. 10

(B) A SPARK implementation has K register windows. What is the number N of physical register ? Explain. 4

9. (A) Explain the difference between hardwired controlled and micro programmed control architecture. 7

(B) An encoded microinstruction format is to be used. Show how a 9 - bit micro operation field can be divided into subfield to specify 46 different actions. 6

OR

10. (A) Define the following terms :-

(i) Micro - Operation.

(ii) Micro - Program. 7

(B) We wish to provide 8 control words for each machine instruction routine. Machine instruction opcodes have 5 bits, and control memory has 1024 words. Suggest a mapping from the instruction register to the control address register. 6

11. (A) With the help of neat diagram Explain multiple processor organization. 7

(B) Define and differentiate between SIMD and MIMD with the help of block diagram. 6

OR

12. (A) Draw and explain Symmetric Multiprocessor organization. 7

(B) Explain :—

(a) Cluster.

(b) Non - Uniform Memory Access.

(c) Vector Computation. 6