AU – 2870

Seventh Semester B. E. (Electronics and Telecommunication Engineering) Examination

VLSI DESIGN

Paper – 7 XT 04

(USC – 10630)

P. Pages : 3

Time : Three Hours] [Max. Marks : 80

Note : (1) Separate answer book must be used for each section in the subject Geology, Engineering material of civil branch and Separate answer book must be used for Section A and B in Pharmacy and Cosmetic Tech.
(2) Answer **Three** questions from Section A and **Three** questions from Section B.
(3) Due credit will be given to neatness and adequate dimensions.
(4) Assume suitable data wherever necessary.
(5) Illustrate your answer wherever necessary with the help of neat sketches.
(6) Use pen of Blue/Black ink/refill only for writing the answer book.

SECTION A

1. (a) Explain advantages and applications of VLSI. 6

   (b) Explain IP life cycle in detail. 7

OR

2. (a) Explain Design and testability for integrated circuit design. 7

   (b) Explain integrated circuit manufacturing. 6

3. (a) Explain VLSI design flow. 6

   (b) Write a VHDL code for ALU using case statement. 7

OR

4. (a) Explain Data types in VHDL. 6

(b) Write down a VHDL program for a circuit. 3:8 Decoder using behavioral style of modelling. 7

5. (a) Write a VHDL code for generation of following clock pulses. 7

(i)

Fig. 5 a-i

(ii)

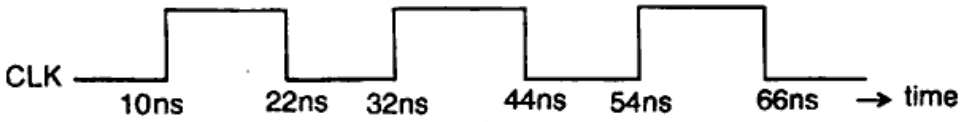

Fig. 5 a-ii 7

(b) How generics are used in VHDL ? Explain in detail with suitable example. 7

OR

6. (a) Write a VHDL code for full adder using structural style of modelling. 7

(b) Explain Generics and configuration in VHDL programming with examples. 7

SECTION B

7. (a) Explain block architecture of CPLD. 7

(b) Explain MAX 7000 Macrocell for ALTERA MAX 7000 CPLD. 7

OR

8. (a) Explain General structure of FPGA. 7

(b) Explain Embedded Array block (EAB) of ALTERA's 10K FPGA. 7

9. (a) Implement following function using CMOS

$$Y = \overline{X_1 \cdot X_2 + (X_3 + X_4) \cdot X_5}$$

where X_1, X_2, X_3, X_4 and X_5 are inputs and Y is the output of circuit. 7

(b) Draw and explain the basic circuit for 3 input NOR Gate using CMOS. 6

OR

10. (a) Explain Tri state logic circuit using CMOS. 6

(b) Explain different power dissipation issues in VLSI. Calculate power dissipation of an inverter if VDD is power supply and C is the load capacitance of inverter. 7

11. (a) Explain Twin Tub Fabrication process of CMOS in detail. 7

(b) Explain λ based design rules for and manufacturing of VLSI circuits. 6

OR

12. (a) Draw Physical layout of NOR Gate using design rules. 6

(b) Explain simulation and synthesis issues in VLSI. 7