B.E. Eighth Semester (Electronics & Telecommu. Engineering) (CGS)

10645: Professional Elective-II: Embedded and Real Time Systems: 8 XT 04

P. Pages: 2 AU - 3002 Time: Three Hours Max. Marks: 80 Notes: 1. Due credit will be given to neatness and adequate dimensions. 2. Assume suitable data wherever necessary. 3. Illustrate your answer necessary with the help of neat sketches. SECTION - A 1. Explain the various characteristics of an Embedded system. 7 a) Explain the components of a typical embedded system. b) OR 2. a) Explain the different classifications of an Embedded system. Give an example for each. b) What is an emulator? What are various components of an emulator? 7 3. Illustrate an semaphore in RTOS. Discuss the types of semaphores with examples. a) List out task states in RTOS. When does a task move from running state to block state? b) OR a) Differentiate between semaphore & mutex. Can counting semaphore be implemented 7 using binary semaphore? 6 b) Explain first cum first serve scheduling in RTOS. 5. a) What are the message queues? How are they different from the events? b) Explain following distinctive characteristics of RTOS. 8 i) Timers Task Priorities ii) iii) Interrupt latency iv) Memory Management. OR What are watchdog timers? How do they help in designing real - time tasks? 6. a)

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b)

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What is meant by memory locking? In which type of environment is it used?

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SECTION - B

7.	a)	Draw and explain block diagram of PIC micro controller. Discuss the need of watchdog Timer.	8
	b)	Differentiate between RISC Vs CISC.	6
OR			
8.	a)	What is THUMB? How does the Thumb instructions set differ from ARM instruction set? Are the THUMB instructions executed directly?	8
	b)	Draw and explain status register of PIC microcontroller.	6
9.		Explain Cyclic and Round Robin with Time Slicing Scheduling model in details.	13
OR			
10.	a)	Explain development process of an Embedded system.	7
	b)	Enlist an application of various software modules and tools for an implementation of Embedded system.	6
11.		Write short note on:	13
		i) I ² CBUS	
		ii) CAN BUS	
OR			
12.		Describe IEEE 11491 (JTAG) testability boundary scan architecture in detail.	13

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