B.E. Sixth Semester (Electronics & Telecommu., Electronics Engg.) (CGS)

10620 : Digital Integrated Circuits : 6 XT 01 / 6 XN 01

P. Pages : 2 | AU - 2774

Time : Three Hours | Max. Marks : 80

* 0 6 1 7 *

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.
4. Use of pen Black ink/refill only for writing the answer book.
5. Mobile phones are not permitted.

1. A) Prove the following Boolean arithmetic equations. **6**

i) $AB + \overline{A}\,C + BC = AB + \overline{A}C$

ii) $(A+B)(\overline{A}+C)(B+C) = (A+B)(\overline{A}+C)$

B) Reduced the function using K-Map and realized the logic circuit using NAND Gate. **8**

$F(A\ B\ C\ D\ E) = \sum m\ (0, 2, 3, 5, 6, 9, 11, 15, 17, 21, 28, 30, 31) + d(12, 20, 23, 24)$

OR

2. A) Reduced the following function using K-Map and realized the logic circuit using NOR Gate only. **7**

$F(A\ B\ C\ D) = \sum m\ (0, 3, 5, 6, 15)$

B) Determine the prime implicants of the function by using Tabular Method. **7**

$F(A\ B\ C\ D) = \sum m\ (0, 1, 3, 4, 6, 7, 8, 9, 10, 11, 12, 15)$

3. A) Design a Full Adder Circuit using 2-Bit 4:1 multiplexer. **6**

B) Implement the following function using 8:1 multiplexer. **7**

$F1(A\ B\ C\ D) = \sum m\ (0, 1, 4, 6, 7, 8, 9, 10, 15)$

OR

4. A) Design a 5-Bit Comparator using only one IC-7485 and logic gate. **6**

B) Design a decimal to BCD encoder and priority encoder and explain the difference between them. **7**

5. Design BCD to seven segment decoder using PLA. **13**

OR

6. A) Give the truth table of IC-7480 and design a 3-bit adder using a IC-7480. **6**

B) Design 4-bit look ahead carry adder and explain its operations. **7**

7. A) Give the characteristics equations for SR, JK, T and D flip-flops. **7**

B) Describe the general models of Sequential machines and explain. 7

OR

8. A) Design state graph for the Mealy model with the sequential input x, D-flip-flops with inputs D_A & D_B, output of the flip-flops are A and B respectively. The output of the circuit is $Z = (A + B)\bar{x}$ 7

The flip-flops input equations are $D_A = A.x + B.x$, and $D_B = x.A$

B) Design a synchronous modulo-4 counter using J-K flip-flops with sequential input x and present state q. 7

9. A) Describe the basic model of asynchronous sequential circuits and explain. 6

B) Draw the asynchronous circuit for the following logic equations and determine transition flow diagram, critical and non critical race occurs in the circuit. 7

$Y1 = x_2' y_1 y_2 + x_2 y_1 y_2' + x_1 y_2' + x_1 x_2 y_1' y_2$

$Y2 = x_1 y_1 + x_2'$

Where x1 & x2 are sequential inputs, y1 & y2 are present states and Y1 & Y2 are the next states.

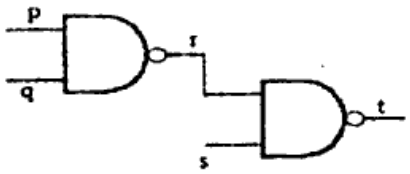
OR

10. A) Design a Moore State Graph for an asynchronous network has two inputs and one output. The input sequence $X_1X_2 = 00, 01, 11$ causes the output to become one. The next input changes then causes the output to return to 0. No other input sequence will produce one output. 7

B) Explain the Hazards in a combinational circuit. 6

11. A) Give the complete test set to detect the fault in a single logic gates OR and AND. 7

B) Find the complete minimal test set for the circuit shown in figure using ENF Method. 6



OR

12. Determine the minimal complete test set for the circuit shown in Fig 12 for s-a-0 and S-a-1 faults. 13

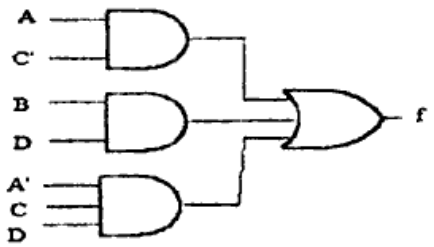


Fig 12

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