AU – 2722

Fifth Semester B. E. (Information Technology) (CGS) Examination

DIGITAL INTEGRATED CIRCUITS

Paper – 5 IT 02

(USC – 10731)

P. Pages : 3

Time : Three Hours] [Max. Marks : 80

Note : (1) Assume suitable data wherever necessary.
(2) Illustrate your answer wherever necessary with the help of neat sketches.
(3) Use pen of Blue/Black ink/refill only for writing the answer book.

1. (A) Convert the equation in sum of Minterm form and implement using only NAND gates :

$F = (xy + z)(xz + y)$ 6

(B) Draw the circuit and explain the operation of TTL NAND gate. 7

OR

2. (A) Convert the equation in canonical POS form and implement using only NOR gates.

$F = xy + \bar{x}z$ 7

(B) Explain following characteristics of digital ICs.

(i) Propagation Delay.

(ii) Noise Margin. 6

3. (A) Minimize using k-map :

$f = \Sigma m(6, 9, 13, 18, 19, 25, 27, 29, 31) + d(2, 3, 11, 15, 17, 24, 28)$ 7

(B) Simplify using k-map and realize the minimized equation using NOR gates.

$F = \pi M(0, 7, 9, 13, 27, 31) \cdot d(2, 4, 8, 18, 30)$ 7

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OR

4. (A) Simplify using k–map and realize using NAND gates.

$f = \Sigma m(0, 1, 5, 6, 8, 9, 11, 13) + d(7, 10, 12)$ 6

(B) Find the PIS and EPI_S, using tabulation method.

$f = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$ 8

5. (A) Implement a full Adder using two Half adder and a logic gate. 6

(B) Realize a function with multilevel NAND circuit.

$f = (\bar{A} + B)(C + DE)$ 7

OR

6. (A) Design and draw a 4–bit binary to Excess–3 code converter. 7

(B) Design and draw a 4–bit odd parity checker. 6

7. (A) Draw and explain a BCD Adder using 4 bit binary adder. 7

(B) Implement a function $f = \Sigma m(0, 2, 5, 6, 9, 11, 14)$ using a 8:1 MUX. 7

OR

8. (A) A combinational ckt is defined by,

$F_1 = \Sigma m(2, 5, 6)$, $F_2 = \Sigma m(1, 4, 5, 7)$ Implement it using a 3:8 decoder and logic gates. 7

(B) Implement the following function with PLA.

$F_1 = \bar{A}\bar{B} + BC$ and

$F_2 = A\bar{C} + BC$ 7

9. (A) Explain how J–K D and T flip flops can be obtained from S–R flip flop. Also give their excitation tables. 6

(B) Design a 4 bit synchronous counter using T–flip flop. 7

OR

10. (A) With the help of truth table draw the state diagram for J–K flip flop. 6

(B) Design and draw a Mod 5 Asynchronous counter. 7

11. (A) Draw a 5 bit shift register that enables the Read and write operations in both serial as well as parallel mode. Explain its function in brief. 7

(B) Draw the structure of static RAM(SRAM) cell and explain its function. 6

OR

12. (A) What are types of RAMs ? Explain in brief. 6

(B) What is ASM ? Explain various blocks of ASM chart. 7