

M.C.A. / P.G.D.C.S. Ist Year First Semester (CGS)
15501 : Computer Organisation : 1 MCA 1

P. Pages : 2

Time : Three Hours



AV - 3263

Max. Marks : 80

- Notes :
1. Assume suitable data wherever necessary.
 2. Illustrate your answer necessary with the help of neat sketches.
 3. Use of pen Blue/Black ink/refill only for writing the answer book.

1. a) Draw and Explain Von Neumann machine architecture in details? 7
b) A program consist of a 100 instruction loop that is executed 42 times. If takes 16,000 cycles to execute the program on-given system, what are that system CPI and IPC values for the program. 7

OR

2. a) Explain the following terms. 7
i) Bus Structure
ii) Execution Unit
b) Explain program development tools with the help of diagram? 7
3. a) What is ALU? Draw & Explain combinational Logic Circuit Based ALU. 7
b) Explain in brief the "Single Precision" method and "Double Precision" method with suitable examples. 6

OR

4. a) Solve the following. Use 8 bit representation of numbers. 7
i) $46 - 14$ (use 1's complement method)
ii) $46 - 14$ (use 2's complement method)
b) What do you mean by Binary Coded decimal? Perform the BCD addition of Od 89 and Od 88. 6
5. a) What do you meant by instruction set? Explain in brief? 7
b) Compare RISC and CISC. 6

OR

6. a) What are different Addressing modes. Explain each.in brief with example. 7
b) What do you mean by input / output instruction? Explain with suitable example. 6

AV - 3263

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7. a) Explain instruction pipeline and its hazards. 7
b) Explain vector processor with suitable diagram. 6

OR

8. a) Explain extracting parallelism in brief. 6
b) Explain in brief the super scalar processor. 7
9. a) What do you mean by Cache memory? Explain Harvard Architecture Cache with suitable diagram. 6
b) Explain semi conductor read-only memories (ROMS) in detail. 7

OR

10. a) Explain the difference between RAM & ROM in term of technology, speed, & size & cost. 6
b) Explain different levels in the memory hierarchy in computer system. 7
11. a) Explain the address translation procedure in virtual memory system with suitable diagram. 7
b) What is Bus Arbitration? Explain with the help of Daisy – Chaining, Polling & independent Requests methods. 7

OR

12. a) Explain demand paging & swapping with suitable diagram. 7
b) Draw & Explain Daisy chaining method. 7
