M.E. First Semester (Electrical & Elect.) (New-CGS)

13284 : VLSI Design : 1 EEEME 4

P. Pages : 2 **AU - 3399**

Time : Three Hours Max. Marks : 80

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.
4. Use of pen Blue/Black ink/refill only for writing the answer book.

SECTION - A

1. a) What is the need of IP based design? What are types of IP? Discuss IP life cycle in detail. **7**

b) Describe the relationship between these design abstraction. **7**
i) Circuit waveforms Vs. digital signals
ii) Digital signals Vs. binary numbers
iii) Logic gates Vs. adders

OR

2. a) Discuss the design and conquer approach of chip design using suitable example. **7**

b) Explain reliability and sources of unreliability with the help of both tub curve. **7**

3. a) Explain domino logic gate structure. Sketch a 3-input dual rail domino OR/NOR gate. **7**

b) Draw and explain pass transistor dc characteristics. What is the drawback of pass transistor and how it is overcome by pass gate? **6**

OR

4. a) Discuss various models used to compute delay and transition time. **7**

b) A 3-input majority gate returns a true output if at least two of the inputs are true. A minority gate is its complement. Design a 3-input CMOS minority gate using a single state of logic. Sketch a transistor level schematic and its stick diagram. **6**

5. a) Give at least one test for stuck at-0 and stuck at –1 faults for each of these static gates: **7**
i) (a+b) (c+d)
ii) [(a+b) c]'

b) What is the Spanning tree and Steiner tree? Explain in brief various methods used for wiring optimizations. **6**

OR

6. a) What is the need of transistor sizing? Explain the theory of logical effort and its related parameters w.r.t. transistor sizing. 7

b) Explain switch logic network using two different styles with an example. 6
i) Constant inputs ii) Non constant inputs

SECTION - B

7. a) Draw the block diagram and explain the use of PLL in clock generation. 7

b) What is clock skew? Is a single phase or two-phase systems mere sensitive to clock skew, justify your answer. 7

OR

8. a) Explain and compare the following methods of sequencing blocks of combinational logic: 8
i) Flip flop based system ii) 2-phase system
iii) Pulsed system

b) What is a clocked inverter? Explain a D-latch built from the clocked inverters and also draw its stick diagram. 6

9. a) Draw and explain the operation of Barrel shifter. 7

b) What are 'active pixel sensors'? Explain the working with neat diagram. 6

OR

10. a) Explain how 3T DRAM is different from 1T DRAM with relevant figures. 7

b) Discuss in detail the image sensor architectures. 6

11. a) Discuss various Techniques that can be used to reduce and manage power consumption. 7

b) Explain the following formats related to floorplanning and placement. 6
i) LEF ii) PDEF

OR

12. a) What is the need of validation during chip assembly. Explain. 6

b) What are the challenges is clock distribution across the chip? Explain H tree and give its advantages. 7

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