M.E. Second Semester (Electrical & Elect.) (New - CGS)

13289 : Embedded Systems Design : 2 EEEME 2

P. Pages : 2 | AU - 3402

Time : Three Hours | Max. Marks : 80

* 1 0 3 4 *

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.

SECTION - A

1. Explain all the instructions of Data Transfer Group for Intel 8051. Also make special comments on MOVC type of instruction. **13**

OR

2. Explain Memory organization available inside architecture of intel 8051. Also provide alternate functions of Port. 3. **13**

3. a) Given an Analog input signal whose voltage ranges from 0 to 19 V and 8 bits for digital encoding for 5 V. Use successive approximation approach to find correct encoding. **7**

b) Four lights are connected to decoder. Build a circuit, that will blink a light in following order 0, 2, 1, 3 ... 0, 2, 1, 3..... start from state diagram, State table, minimize the logic and draw the final circuit. **6**

OR

4. a) Determine the values for TH1 to generate a baud rate of 9600 BPS for 8051, Assuming 11.0592 MHz oscillator. Take two values of SMOD as 0 and 1. **6**

b) Design a single purpose processor that outputs Fibonacci numbers upto n places. Start with a function computing the desired result, translate it into a state diagram & sketch a probable datapath. **7**

5. a) Draw block diagram of arbitration using daisy chain configuration. **6**

b) With example, illustrate how to compose large memory from small memory. **8**

OR

6. Assume an 8051 is used as a master device on an I2C bus with P1.0. corresponding to I2C_Data and pin P1.1 corresponds to I2C_clock. Write a set of C routines that encapsulate the details of I2C protocol. Specifically, write the routines called start I2C/ Stop I2C, that send the appropriate start/stop signal to slave devices. Likewise, write the routines read Byte and write Byte, each taking a device I_d as input and performing the appropriate I/O actions. **14**

SECTION - B

7. a) Explain architecture of programmable logic device FPGA. How it is programmed? **7**

   b) Explain different models required to describe Embedded system with suitable example. **6**

OR

8. a) List and describe three general approaches to improve designer productivity. **6**

   b) Explain FSM and concurrent process with suitable example. **7**

9. Given the process A through F in table, where their deadline equals their period. Determine whether they can be scheduled on time using non preemptive scheduler. Assume all processes begin at the same time and their execution times are as follows : **14**
   A = 8 ms, B = 25 ms, C = 6 ms, D = 25 ms, E = 10 ms, F = 25 ms.

Process	Period (ms)	Priority
A	25	5
B	50	3
C	12	6
D	100	1
E	40	4
F	75	2

Table Qu. 9.

Explain your answer by showing that each process either meets or misses its deadline.

OR

10. a) Explain interrupt routines in RTOS environment. **6**

    b) Explain with suitable example, how Semaphores are used to solve shared data problem. What are counting Semaphores? **8**

11. Explain various features of Linux that are useful for embedded system design. **13**

OR

12. In relation to embedded Linux, how TCP/IP networking is done? Explain network configuration. **13**

****