www.sgbauonline.com

M.Sc. Second Semester (Applied Electronics) (New) (CBS)

15018 : Digital Integrated Circuits : 2 AE 3

P. Pages : 2

Time : Three Hours

* 0 8 7 4 *

AU - 3183

Max. Marks : 80

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.

1. a) Prove that 6

i) $\overline{\overline{AB}+\overline{A}+AB}=0.$

ii) $A\overline{B}C+\overline{A}BC+ABC=AC+AB$

b) Reduce following & realize using NOR gates only. 8

$f=\pi M(0,3,7,8,9,10,11,15)\cdot d(2,4).$

OR

2. a) Prove Do Morgan's theorem. 6

i) $\overline{AB+CD}=\overline{AB}\cdot\overline{CD}$

ii) $\overline{(A+B)\cdot(C+D)}=\overline{(A+B)}+\overline{(C+D)}$

b) Minimize following using K-map & realize using NAND gates. 8

$f(A,B,C,D)=\sum m(8,9,10,11,13,15,16,18,21,24,25,26,27,30,31).$

3. a) Draw & Explain TTL totem pole NAND gate. 7

b) Explain CMOS NOR gate with suitable diagram. 6

OR

4. a) Convert R-S FF into JKFF. 6

b) Explain shift Register with suitable diagram. 7

5. a) Design 8:256 decoder using 4 : 16 decoder. 7

b) Implement following using multiplexer. 6

$f(A,B,C,D)=\sum m(0,2,3,6,8,9,12.14).$

OR

6. a) Design a 16 bit odd parity checker using IC 74180. 7

b) Explain BCD to 7-segment decoder/driver IC 7447. 6

www.sgbauonline.com

www.sgbauonline.com

7. a) Implement following using PLA 7

$F_1 = \overline{A}BC + A\overline{B}C + A\overline{C}$

$F_2 = \overline{A}\overline{B}\overline{C} + BC$

b) Explain How ROM is used as PLD. 7

OR

8. a) Explain in detail FPGA using suitable diagrams. 7

b) Explain carry look ahead adder. 7

9. a) Classify the semiconductor memories. 7

b) Explain a CMOS SRAM memory cell. 6

OR

10. a) Using intel 2716 2kx8 EPROM obtain 7
i) 4kx8 ROM.
ii) 2k x 16 ROM.

b) Explain the CCD memory. 6

11. a) Explain moose and Mealy models of sequential machine. 6

b) Obtain state diagram & state table for 7
i) JKFF ii) TFF

OR

12. A sequential circuit has two JKFFA & B, two inputs x and y and are output z. 13
The FF input equation and output equation are

$J_A = Bx + \overline{B}\overline{Y}$ $K_A = \overline{B}x\overline{Y}$

$J_B = \overline{A}x$ $K_B = A + x\overline{Y}$

$z = A\overline{X}\overline{Y} + B\overline{X}\overline{Y}$.

i) Draw logic diagram 9 ckt.
ii) Tabulate the state table.
iii) Derive state equation for A and B.

****

www.sgbauonline.com