M.Sc. (Part—I) Semester—II (CBCS Scheme) Examination
2-ELE3 : ELECTRONICS
(Digital IC's and Design)
Paper—VII

Time : Three Hours] [Maximum Marks : 80

Note :— (1) **All** questions are compulsory.

(2) Draw sketches wherever necessary.

EITHER

1. (a) Explain Minterm and Maxterm. 8

(b) Explain POS. 4

(c) Explain Quine McCluskey method. 4

OR

(p) Explain synthesis of OR gate by using NAND gate. 8

(q) Explain SOP. 4

(r) What are Boolean rules ? Give any two examples. 4

EITHER

2. (a) Explain Decimal to BCD encoder using IC 74147. 8

(b) Draw diagram of 3 : 8 line decoder. 4

(c) What is parity ? Explain with example. 4

OR

(p) Explain 4 : 1 MUX with logical diagram and truth table. 8

(q) Explain 1 bit magnitude comparator. 4

(r) What are comparators ? 4

EITHER

3. (a) Explain 4 bit binary adder/subtractor using IC 7480. 8

(b) Explain Full adder using two half adders. 8

OR

(p) Explain PLA and PAL. 8

(q) Explain combinational logic design using ROM array. 8

EITHER

4. (a) Explain SM chart in detail. 8

(b) Explain equivalence and minimization network with example. 8

OR

(p) What is state assignment ? Explain its rules. 8

(q) Give the detailed analysis of clocked sequential network. 8

EITHER

5. (a) Explain the analysis of asynchronous sequential network. 8

(b) State assignment and realization of flow tables. 8

OR

(p) Explain derivation and reduction of primitive flow tables. 8

(q) Explain different hazards in sequential network. 8