

AU-323

M.Sc. (Part—I) Semester—II (CBCS Scheme) Examination

ELECTRONICS INSTRUMENTATION

Paper—VII

2-ELE3 : Digital IC's and Design

Time : Three Hours]

[Maximum Marks : 80

1. (a) Explain the following terms :
 - (i) Two variable map.
 - (ii) Three variable map. 4
- (b) Explain DeMorgan's theorem for three variable with logical diagram and truth table. 6
- (c) What is SOP and POS standard logical function ? Explain it with example. 6

OR

- (p) Explain Don't care condition with example. 5
- (q) Solve the following using Kmap :

$$F(x, y, z) = \Sigma(2, 3, 4, 5).$$
 5
- (r) Design any six Boolean rules for AND & OR Operation. 6
2. (a) Explain 1:8 Demultiplexer using AND logic gate with truth table. 6
- (b) What is code converter ? 4
- (c) Explain 4:16 Decoder. 6

OR

- (p) Explain parity generator and parity checker. 6
- (q) What is encoder ? Give its application. 4
- (r) Explain BCD to 7 Segment decoder. 6

3. (a) Explain ROM array in brief. 8
 (b) What is PLA ? Explain it in brief. 8

OR

- (p) Explain PAL with truth table. 8
 (q) Explain 4 bit adder subtracter with examples. 8
 4. (a) Explain MSJK flip-flop with truth table. 7
 (b) Explain Race around condition in JKFF. 3
 (c) Design mod-16 counter with JKMSFF and give its truth table & waveform. 6

OR

- (p) Explain the general model of sequential machines. 6
 (q) What is D-Latch ? 2
 (r) Explain 3-bit asynchronous up-down counter with truth table & waveform. 8
 5. (a) Design 5-bit shift register using RSFF with its waveform. 8
 (b) Explain the concept of Ring-counter. 8

OR

- (p) Explain derivation and reduction of primitive flow table. 8
 (q) Explain asynchronous sequential network design. 8