M.Sc. Third Semester (Applied Electronics) (New) (CBS)

15037 : VLSI Design : 3 AE 3

P. Pages : 2 | AU - 3191

Time : Three Hours | Max. Marks : 80

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.
4. Use of pen Blue/Black ink/refill only for writing the answer book.

SECTION - A

1. a) What is meant by Hazard Free digital circuits? How is it realized? Explain with an example. 7

b) Simplify the following function using K-map technique. 7

$F(A,B,C,D) = \Sigma_m (5,6,7,12,13) + \Sigma_d (4,9,14,15)$

OR

2. a) Design and draw the logic circuit for binary code to gray code conversion. 7

b) Using tabulation method simplify the Boolean function 7
$F(W,X,Y,Z) = \Sigma(2,3,4,6,7,11,12,13,14)$ which has don't care conditions $d(1,5,15)$.

3. a) Compose a behavioral VHDL description of a ÷ 5 counter without using variables. Use synchronous reset. 7

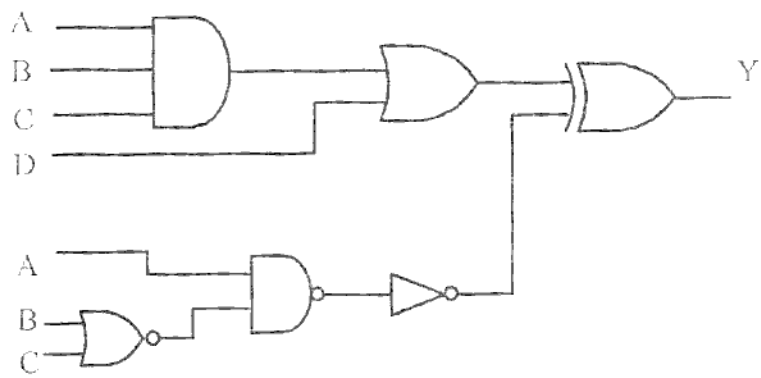
b) Design and develop a VHDL code to 8 : 3 encoder. 6

OR

4. a) Illustrate the data objects used in VHDL with suitable examples. 6

b) Compose a VHDL code for 8 bit ALU in data flow modeling. 7

5. a) Develop a VHDL code for the given circuit in component logic. 7



b) Compose a VHDL code for positive edge function as declared in package. 6

OR

6. a) Define attributes and explain any two signal attributes supported by VHDL. 7

b) Contrast VHDL with an ordinary programming language. 6

SECTION - B

7. a) Explain in detail configuration logic block of FPGA. 7

b) Explain Switch matrix in CPLD. 7

OR

8. Draw a neat block diagram and explain the CLBs and IOBs of Xilinx 4000 series FPGA. Also highlight the boundary scan logic in IOB. 14

9. a) Describe DC characteristics of CMOS as inverter. 7

b) Explain various sources of power dissipation in CMOS circuits. 6

OR

10. a) Design CMOS logic for the following functions 7

i) $A \cdot \overline{B + C \cdot (\overline{A + B})}$

ii) $\overline{\overline{A \cdot B} + A \cdot B}$

b) Explain different delays associated with CMOS circuits. 6

11. a) Define the terms : 6

i) Oxidation

ii) Epitaxy

iii) Deposition

b) Draw the physical layout of 2 input NAND and NOR gates using CMOS logic. 7

OR

12. Explain with neat diagrams the various CMOS fabrication technology. 13

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