AR–2543

Faculty of Engineering & Technology

M.Sc. (Applied Electronics) Semester—III (New) (C.B.S.) Examination

VLSI DESIGN

(15037)

Paper—3 AE 3

Sections—A & B

Time : Three Hours] [Maximum Marks : 80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Answer **THREE** questions from Section A and **THREE** questions from Section B.

(3) Due credit will be given to neatness and adequate dimensions.

(4) Assume suitable data wherever necessary.

(5) Illustrate your answers wherever necessary with the help of neat sketches.

(6) Use pen of Blue/Black ink/refill only for writing the answer book.

SECTION—A

1. (a) Design a hazard free ckt. in AND-OR configuration for the logic function.

Y (A, B, C, D) = Σm (1, 3, 5, 7, 12, 13). 7

(b) Explain Moore model of sequential machine. 6

OR

2. (a) Minimize the logic function using Quine McCluskey method

f (A, B, C, D) = Σm (2, 4, 8, 11, 15) + d(1, 10, 12, 13). 8

(b) $F = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$

Express F in canonical SOP form. 5

3. (a) Explain data types with suitable example. 4
   (b) Explain process statement with suitable example. 4
   (c) Give the dataflow VHDL description of an EX-OR gate. 6

OR

4. (a) Explain data objects in VHDL with suitable example. 4
   (b) Describe 4 : 1 MUX using if statement. 4
   (c) How does a hardware description language like VHDL differ from an ordinary programming language ? 6
5. (a) What is generics ? Explain with suitable example. 7
   (b) Describe 4 bit binary counter using structural modelling. 6

OR

6. (a) What are 'attributes' ? Explain any two signal attributes supported in VHDL. 7
   (b) Explain the use of IEEE library in VHDL. 6

SECTION—B

7. (a) Explain the features of typical CPLD and give comparison between CPLD and FPGA. 8
   (b) What are the advantages and disadvantages of antifuse FPGA ? 6

OR

8. (a) Draw a neat block diagram and explain the CLBs and IOBs of Xiling 4000 series FPGA. 9
   (b) Compare Altera and Xiling FPGA. 5
9. (a) Compare TTL, MOS, and CMOS logic. 7
   (b) Explain power dissipation regarding CMOS. 6

OR

10. (a) Draw and explain the basic CMOS layout of an inverter. 7
    (b) Draw the CMOS logic diagram of three input Nand gate. 6
11. (a) Explain the P-well CMOS fabrication process in short. 7
    (b) Explain λ rule for CMOS fabrication. 6

OR

12. (a) What is test bench ? Write test bench for AND gate. 7
    (b) Explain twin tub process in CMOS with suitable diagram. 6