M.Sc. Part-II (Semester-III) (C.B.C.S.) Examination

PHYSICS

Paper—3PHY4 (i) Digital Techniques

Time : Three Hours] [Maximum Marks : 80

Note :— (1) **ALL** questions are compulsory.
(2) All questions carry equal marks.

1. (A) Compare different performance parameters of various logic families. 6

   (B) Draw a circuit of 2-input RTL, TTL NAND gate and find the truth table. 6

   (C) Explain why CMOS is preferred. 4

OR

   (P) Draw a circuit of NMOS NAND gate. Explain construction and working of it. Write its truth table. 6

   (Q) Explain how a transistor could be used as logic switch. 4

   (R) Show that NAND gate can be used as universal logic gate. 6

2. (A) How quad in K-map eliminates two variables and their compliments ? Explain it with suitable example. 6

   (B) Explain the working of 4-bit Adder-2-Subtractor Circuit using 7483 and 7486. 6

   (C) Show that complement of sum is product of complement using appropriate logic diagrams. 4

OR

   (P) How pair in K-map eliminates one variable and its compliment ? Explain it with suitable example. 4

   (Q) Obtain the combinational logic design circuit for 4-bit multiplier using 7483 and 7408 ICs. 6

   (R) Use K-Map to find the simplest circuit for Full Adder. 6

3. (A) Explain with the help of circuit using basic gates the operation of 2-Bit ALU which can perform following operations. Explain also the selection circuit for the desired operation.

   (i) F = Complement of A

   (ii) F = A and B

   (iii) F = A exor B

   (iv) F = A plus B. 12

(B) What are multiplexers and De-multiplexers ? With circuit diagram using basic gates explain 2 : 1 line multiplexer and 1 : 2 demultiplexer operation. 4

OR

(P) Explain the working of IC 7447 BCD to SSD Decoder with the block diagram and external circuit for SSD (Common Anode) and determine the 8-bit codes for display of 3, 7, 9 and 1 on the same. 12

(Q) Define encoder and decoder. Explain 74138 (3 : 8 decoder) operations. How one can realize the same with 1 : 8 DEMUX ? 4

4. (A) Draw detailed diagram of master slave flip-flop and label it. 4

(B) Determine the number of flip-flops needed to construct a shift register capable storing (a) decimal number upto 32, (b) hexadecimal number upto F. 4

(C) Explain working of 7493 with timing diagram. 4

(D) Explain control buffers. 4

OR

(P) How can R.S. Flip-flop be constructed by using NOR gate, explain its working. 4

(Q) Explain the working of 4-bit serial in-serial out shift register with neat logic diagram. 4

(R) Draw and logic diagram of a ring counter and explain its working. 4

(S) Obtain modulo 6 up counter using JKMSFF. 4

5. (A) Draw logic diagram of 1-bit memory cell using DFF and explain its various functions. Explain the concept of serial expansion and parallel expansion and obtain a 4 × 4 memory organization using 1-bit memory cell. 12

(B) Explain the terms SRAM, DRAM. Illustrate the differences and specific features of these memories. 4

OR

(P) Using IC 6264 (8 KB) and 74138 obtain memory organization 64 KB. 12

(Q) Distinguish between Volatile and Non-volatile NMOS memory cell. 4